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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/584,994
Filing Date: June 29, 2006
Appellant(s): BAIRO, MASAAKI

Ronald P. Kananen
Christopher M. Tobin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09 September 2008 appealing from the Office action mailed 22 February 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

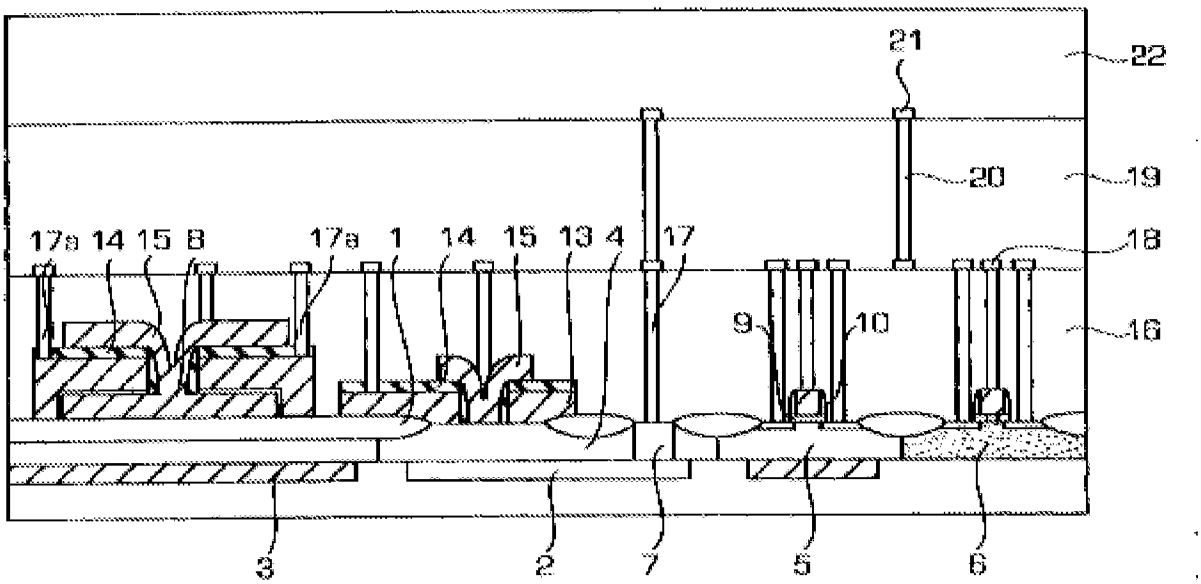
Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii (US 6,307,227) (hereinafter Fujii) in view of Hozumi (US 5,013,677) (hereinafter Hozumi), and further in view of Morimoto (US 6,885,081) (hereinafter Morimoto).

With respect to claim 9, Fujii (e.g. Figure 10) teaches a method for manufacturing a bipolar transistor, the method comprising the steps of:

- Forming a base layer 13 on an insulator 1, said base layer being in contact with a portion of a semiconductor substrate (2, 4; 30 Figure 3);
- Forming an insulating film 16 on said base layer 13;
- Forming base and emitter electrode lead openings within said insulating film 16 (column 8, lines 27-30);
- Depositing a conducting film (polysilicon) into said base electrode lead opening and into said emitter electrode lead opening, said conducting film within said

base electrode lead opening being a base electrode lead portion and said conducting film within said emitter electrode lead opening being an emitter electrode lead portion (column 8, lines 27-30)

FIG. 10



Fujii fails to teach that the base electrode lead opening is formed simultaneous with the emitter electrode lead opening. Fujii further fails to teach a step of polishing the conducting film to separate the base electrode lead portion from the emitter electrode lead portion. Hozumi teaches that the base electrode lead opening is formed simultaneous with the emitter electrode lead opening (column 6, lines 57-61) in order to realize the simultaneous production of a transistor and other elements with a simplified process of manufacture (column 7, lines 67-68; column 8, lines 1-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the method of Fujii with the step of simultaneously forming the base and electrode lead openings as taught by Hozumi for the benefit of

realizing the simultaneous production of a transistor and other elements with a simplified process of manufacture.

Fujii as modified by Hozumi further fails to teach a step of polishing the conducting film to separate the base electrode lead portion from the emitter electrode lead portion. Morimoto teaches a step of polishing a conducting film to separate electrode lead portions in order to form individual plugs in via holes (column 6, lines 17-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the method of Fujii as modified by Hozumi with the polishing step of Morimoto for the benefit of forming individual plugs in via holes.

With respect to claim 10, Fujii (e.g. Figure 10) teaches that said insulator 1 is on said semiconductor substrate (2, 4; 30 Figure 3) with an opening within said insulator exposing said portion of the semiconductor substrate.

With respect to claim 11, Fujii teaches that the base layer 13 is a semiconductor material (column 4, line 37).

With respect to claim 12, Hozumi (e.g. Figure 2C) teaches that the conducting film 11 is deposited simultaneously into said base and emitter electrode lead openings (column 5, lines 31-35).

With respect to claim 13, Hozumi (e.g. Figure 2H) teaches the step of diffusing a dopant 16e from said emitter electrode lead portion into said base layer 7 to form an emitter region with said base layer.

Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii as modified by Hozumi and Morimoto as applied to claim 9 above, and further in view of Besser et al. (US 2003/0235984) (hereinafter Besser).

With respect to claim 14, Fujii as modified by Hozumi and Morimoto teaches all of the limitations of claim 9 above.

Fujii as modified by Hozumi and Morimoto fails to teach a step of depositing a silicide onto a polished surface of said conducting film (*however, note that Fujii teaches the step of depositing aluminum on the surface of the conducting film; column 8, lines 39-40). Besser teaches that it is advantageous to use silicide instead of aluminum in order to provide contacts that are reliable, thermally stable, and have lower resistivity [0003].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the method of Fujii with the silicide of Besser for the benefit of providing contacts that are reliable, thermally stable, and have lower resistivity.

With respect to claim 15, Fujii (e.g. Figure 10) teaches a step of depositing an interlayer insulator 19 onto said silicide and said insulating film.

(10) Response to Argument

With respect to Applicant's response to the rejection of claims 9-15, initially, and in response to applicant's arguments against the references individually, it is noted that

one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Response to Arguments regarding claims 9-13:

Regarding Applicant's response that "Fujii fails to disclose, teach, or suggest forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening" (Appeal Brief at page 6), it is noted that Fujii teaches forming base and emitter electrode lead openings (holes) within said insulating film 16 (Fujii at column 8, lines 27-30), and Hozumi teaches the missing limitation that the base electrode lead opening 9b is formed simultaneous with the emitter electrode lead opening 9e (Hozumi at column 6, lines 57-61) for the benefit of realizing the simultaneous production of a transistor and other elements with a simplified process of manufacture (Hozumi at column 7, lines 67-68 – column 8, lines 1-10).

Regarding Applicant's response that "Hozumi fails to teach the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion" (Appeal Brief at page 7), it is noted that Morimoto teaches a step of polishing a conducting film to separate electrode lead portions for the benefit of forming individual plugs in via holes (Morimoto at column 6, lines 17-25).

Regarding Applicant's response that "Morimoto fails to teach surface polishing by the CMP method to separate one portion 14 from another portion 14" (Appeal Brief at page 7), it is noted that a titanium nitride film and a tungsten film are deposited on the surfaces of the via hole to provide a state where the via holes are filled. Then, surface polishing by the CMP method is performed starting with the surface of the tungsten film 14 to remove the tungsten and titanium nitride films *other than the film portions filled in the via holes, whereby a plug 14* (same reference number as that for the tungsten film is used for the sake of convenience) made of titanium nitride film and the tungsten film 14 *is formed in each via hole 13, as shown in Fig. 2C* (Morimoto at column 6, lines 11-24). Since the titanium nitride and tungsten films are deposited on and in the via holes 13 (providing a state where the via holes are initially connected through surface layer 14) and then subsequently CMP polished to leave only plugs 14 in the via holes, Morimoto teaches surface polishing by the CMP method to separate one portion 14 from another portion 14.

Regarding Applicant's response that "Morimoto fails to teach the presence of a bipolar transistor" but instead, "the figures of Morimoto depict a capacitor" (Appeal Brief at page 7), it is noted that primary reference Fujii (e.g. Figure 10) teaches the presence of a bipolar transistor with separate base and electrode lead portions (Fujii at column 8, lines 27-30). Fujii fails to teach how the base and electrode lead portions of the bipolar transistor are separated. Morimoto teaches *a step of polishing a conducting film to separate electrode lead portions* for the benefit of forming individual plugs in via holes (Morimoto at column 6, lines 17-25). Thus, the combination of Fujii in view of Hozumi,

and further in view of Morimoto teaches the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.

Response to Arguments regarding claims 14 and 15:

With respect to Applicant's response to the rejection of claim 14, arguing each of Fujii, Hozumi, Morimoto, and Besser individually (Appeal Brief at pages 10-12), it is noted that the combination of Fujii in view of Hozumi, and further in view of Morimoto teaches all of the limitations of claim 9, from which claim 14 depends. Fujii as modified by Hozumi and Morimoto fails to teach a step of depositing a silicide onto a polished surface of said conducting film (*however, note that Fujii teaches the step of depositing aluminum on the surface of the conducting film; Fujii at column 8, lines 39-40). Besser teaches that it is advantageous to use silicide instead of aluminum in order to provide contacts that are reliable, thermally stable, and have lower resistivity (Besser at paragraph [0003]). Thus, the combination of Fujii as modified by Hozumi, Morimoto, and Besser teaches depositing a silicide onto a polished surface of said conducting film.

With respect to Applicant's response to the rejection of claim 15, arguing that Fujii fails to teach "the step of depositing an interlayer insulator onto said silicide and said insulating film" because Fujii at column 8, lines 39-41 teaches that "a first wiring layer 18 is formed with aluminum or the like" (Appeal Brief at page 14), it is noted that Besser teaches that it is beneficial to substitute silicide for aluminum in order to provide contacts that are reliable, thermally stable, and have lower resistivity (Besser at paragraph [0003]). Thus, the combination of Fujii as modified by Hozumi, Morimoto,

and Besser teaches the step of depositing an interlayer insulator onto said silicide and said insulating film.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/W. Wendy Kuo/

Examiner, Art Unit 2826

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/Sue A Purvis/
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